REMARKS

Claims 1-16 are pending in the subject patent application and, of those claims, claims 7-11 and 13 are allowed. The allowance of these claims is acknowledged with appreciation.

Claims 1-6, 12 and 14-16 are rejected under 35 USC 112, second paragraph, as being indefinite. In particular, the Examiner alleges that the phrase "one dimension of the transistor" in claims 6 and 12 is vague. The Examiner further alleges that the phrase "creating an imbalance" in claim 14 is vague and that "the signal transistor" in claim 1 lacks antecedent basis. The foregoing rejections are respectfully disagreed with, and are traversed below.

While not admitting that claims 1, 2, 6 and 14 are in any way vague or indefinite, these claims have been further clarified to improve upon the wording. In particular, "signal" has been changed to "input" in claims 1 and 2. Claim 6 has been amended to recite, in part, that "at least one channel dimension of the transistors of the set of transistors differs from a channel dimension of at least two of transistors of the set of transistors." Similarly claim 12, which depends from allowed claim 7, has been amended to recite, in part, that "at least one channel dimension of the transistors of the set of parallel-connected transistors differs from at least one channel dimension of the other transistors of the other set of parallel-connected transistors." Claim 14 has also been clarified to recite, in part, "means for creating an offset in said quantizer input transistors that results in the generation of a desired pseudo-noise dither signal at said input to said quantizer."

In view of the foregoing, the Examiner's 35 USC 112, second paragraph, rejection of claims 1-6, 12 and 14-16 should be reconsidered and withdrawn.

Lastly, claims 1-2 and 5 are rejected under 35 USC 102(b) as being anticipated by US Patent No. 5,790,063 to Koifman et al. This rejection is respectfully disagreed with, and is traversed for the following reasons.

Independent claim 1 is directed to a method to generate a dither signal in a sigma-delta

modulator, comprising:

at an input of a quantizer, dividing at least one input transistor into a set of transistors connected together in parallel;

generating a digital signal having random or pseudo-random characteristics; and

activating individual transistors of the set of transistors with the digital signal to generate a noise signal that is added to an output of the input transistor.

The Koifman et al. reference is directed to an analog-to-digital converter on CMOS with MOS capacitor. According to this reference, the dithered input signal to the comparator consists of two separately created current mode components: one current mode component created from the signal in the AD converter and a second current component containing the dither and created with separate current sources. The signal current and dither currents are created separately by separate transistors and added together by connecting the outputs of the transistors together.

In contrast, according to embodiments of the subject invention, the dither is created by causing artificial time varying mismatch in the input transistors to the comparators. In this method, a separate dither current or voltage does not exist. In further accordance with embodiments of the invention, dithering is created by artificially disturbing the voltage to current conversion in the input of the quantizer. The voltage to current conversion gain is artificially made imprecise and time varying by creating artificial time varying offset. This artificial time varying mismatch or offset in the voltage to current conversion is created by having the input transistors split or divided into a plurality of transistors (a set of transistors) connected in parallel and then activating or deactivating the individual transistors in pseudo-random fashion (see claim 1).

Moreover, Applicants respectfully note that Figs. 9A, 9B and 13 of Koifman et al. are employed by the Examiner in this anticipation rejection. However, if the Examiner is using the parallel transistors of Fig. 13 in rejecting claim 1, it is respectfully noted that these transistors (some of which receive the dither signals) are part of the current sources 554, 553,

etc. of Fig. 9A. In Fig. 9A, the input is 505, 605 and the VIC is a voltage-to-current converter. Transistors 526, 527 (and 626, 627) that follow the VIC do not appear to be connected in parallel, as one feeds the switch bank and the other feeds the reference current block.

The Examiner is respectfully reminded that for a rejection to be made on the basis of anticipation, it is well recognized that "to constitute an anticipation, all material elements recited in the claim must be found in one unit of prior art," *Ex Parte Gould*, BPAI, 6 USPQ 2d, 1680, 1682 (1987), citing with approval *In re Marshall*, 578 F.2d 301, 304, 198 USPQ 344, 346 (CCPA 1978). In the instant case, it should be clear that the disclosure of Koifman et al. does not anticipate nor suggest the claimed invention.

For at least the reasons set forth above, independent claim 1 should be found be allowable. In that claim 1 is clearly in condition for allowance, then claims 2 and 5 should also be found to be allowable in view of their dependency from an allowable independent claim.

All issues raised by the Examiner having been addressed, the subject patent application is believed to be in condition for immediate allowance. Accordingly, the Examiner is respectfully requested to reconsider and remove all of the outstanding rejections and to pass this patent application to issuance.

Respectfully submitted:

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